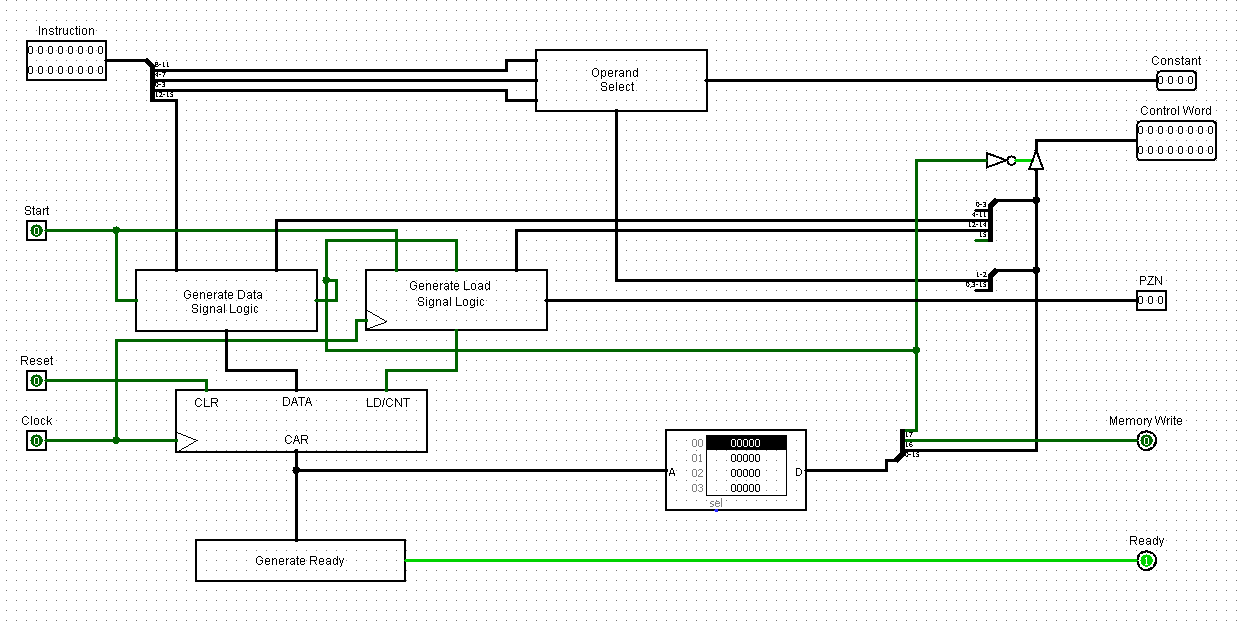
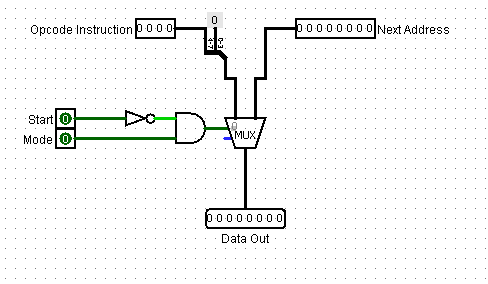
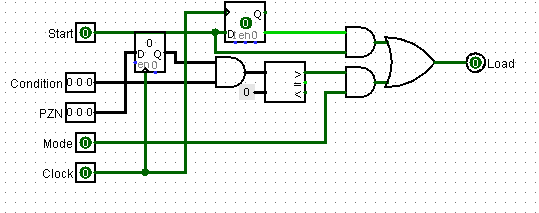
Control Unit



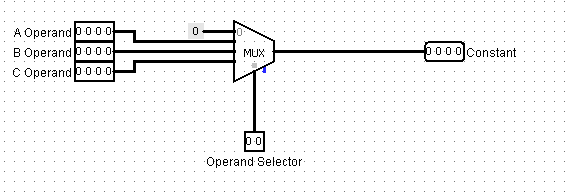
Generate Data Signal Logic



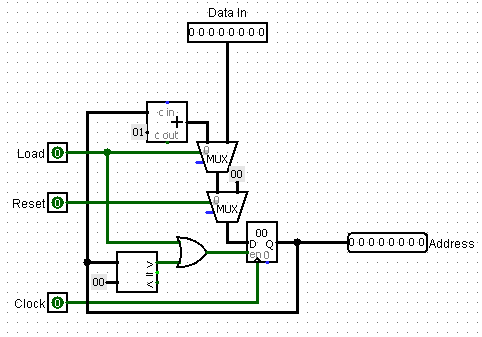
Generate Load Signal Logic



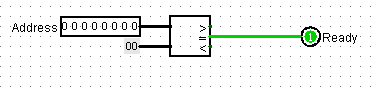
Operand Select



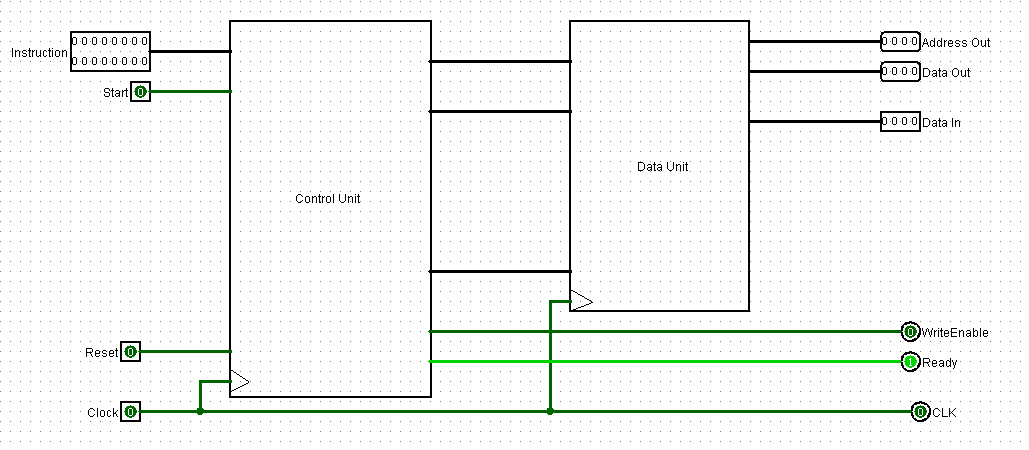
Control Address Register



Generate Ready



Microprocessor



Structural Overview

